AMENDMENTS TO THE CLAIMS

Applicants have canceled Claims 3, 14-15, and 17 without prejudice. Applicants have amended Claims 1, 4-6, and 16 in the following listing, in which added text is underlined and deleted text is stricken-through. The listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently amended) A real-time three-dimensional image processing system comprising:

an optical axis control means for controlling an optical axis angle of left and right cameras by far and near distances of a subject;

an image processing unit for temporarily storing digital image signals of the left and right cameras and converting an analogue image signal into a digital, thereby respectively outputting the digital image signals;

an image matching unit for calculating a decision value representing a minimum matching cost from the left and right digital image signals and then for outputting a disparity value according to the decision value; and

first and second memory devices for alternately storing the decision value,

wherein the image matching unit comprises:

left and right image registers for respectively storing image signals of the left and right cameras;

a processing means for calculating the decision value from images inputted from the left and right image registers by a clock signal and then for outputting the disparity value;

an input/output decision value buffer for alternately exchanging the decision value with the first and second memory devices from an external selection signal; and

a control unit for controlling the processing means by using setting signals which set a register value of the processing means by receiving an external control signal.

2. (Original) The system of claim 1, further comprising a display means for displaying image that processed in accordance with the disparity value.

3. (Canceled).

4. (Currently amended) The system of claim ~~3~~ 1, wherein the setting signals comprises a top signal for activating the uppermost processing means among the processing means in a range of the disparity value; a bottom signal for activating the lowermost processing means among the processing means in a range of the disparity value; a base signal for activating a processing means placed at a position having a disparity `0` among the processing means in a range of the disparity value; and a reset signal for initializing the processing means~~;~~.

5. (Currently amended) The system of claim ~~3~~ 1, wherein the decision value buffer alternately stores the decision value calculated from the processing means in the first memory device or the second memory device, and reads the decision value from the first and second memory devices alternately to output to the processing means.

6. (Currently amended) The system of claim ~~3~~ 1, wherein the processing means comprises:

a forward processing means for calculating a matching cost by receiving a pixel of a scan line stored at the image register and then for outputting the calculated decision value to the decision value buffer; and

a backward processing means controlled by the base and the reset signals for outputting a disparity value by receiving the decision value (Dbin) from the decision value buffer.

7. (Original) The system of claim 6, wherein the decision value outputted from the forward processing means is inputted to the decision value buffer means, and the decision value outputted from the decision value buffer means is inputted to the backward processing means.

8. (Original) The system of claim 6, wherein the forward processing means comprises:

a path comparison means for calculating a matching cost by a difference of each pixel of the scan lines outputted from the left and right image registers, adding the matching cost to an accumulated cost which is fed-back from a accumulated cost register, and receiving the added cost, an accumulated cost of the uppermost processing means, and an accumulated cost of the lowermost processing means by a setting of the top and bottom signals, thereby outputting the minimum cost among the three costs; and

an accumulated cost storage means for storing the minimum cost as an entire cost and adding the entire cost to an occlusion cost, thereby outputting the added cost to an adjacent processing means.

9. (Original) The system of claim 8, wherein the path comparison means comprises:

an occlusion comparison means for receiving the uppermost and the lowermost costs by comparing the inputted three costs, selecting the lowermost cost when the top signal notifying the uppermost processing means is activated, selecting the uppermost cost when the base signal notifying the lowermost processing means is activated, and selecting the minimum cost among the inputted costs in other cases; and

a comparator for selecting a cost which is neither the uppermost cost nor the lowermost cost among the three inputted costs and the minimum cost among the costs outputted from the limitation setting means.

10. (Original) The system of claim 8, wherein the cost storage means comprises:

a D-flip flop which is set or cleared; and

a demultiplexer for setting or clearing the D-flip flop according to a base signal by receiving the reset signal.

11. (Original) The system of claim 8, wherein when the reset signal is activated, the accumulated cost storage means gets the accumulated cost storage means of the processing means having an active base signal have a smaller value than the accumulated cost storage means of the rest processing means.

12. (Original) The system of claim 6, wherein the backward processing means comprises:

a first demultiplexer for outputting the reset signal to a reset of an activated register or a set according to a base signal by receiving the reset signal;

an active register composed of D-flip flops which are set or reset by a control of the first demultiplexer;

an OR gate for receiving active bits, adding the active bits logically, and outputting to the active register;

a second demultiplexer for outputting an output value of the active register according to the decision value; and

a tri-state buffer for outputting the decision value by a control of the active register.

13. (Original) The system of claim 12, wherein when the reset signal is active, the active register activates only an active register of the processing means in which the base signal is active.

14. (Canceled).

15. (Canceled).

16. (Currently amended) A method for a real-time three-dimensional image processing system comprising the steps of:

controlling optical axis values of left and right cameras for an optimum observation and an efficient image matching by far and near distances of a subject;

digitally-converting image signals of the left and right cameras; and

calculating a decision value from the digitally converted image signals of the left and right cameras and then outputting a disparity value by the decision value,

wherein the step of outputting further comprises a step of alternately storing the decision value to the first and second memory devices or alternately reading the decision value from the first and second memory devices.

17. (Canceled).

18. (Original) The method of claim 16, wherein the step of outputting further comprises the steps of:

receiving the digitally-converted image signals, calculating the decision value (Dbin), and

storing the decision value (Dcout) to the first memory device; and

calculating a disparity value by using the stored decision value.

19. (Original) The method of claim 18, further including the steps of:

receiving next image signals, calculating a decision value, and storing the decision value into the second memory device; and

calculating a disparity value by using the stored decision value.

20. (Original) The method of claim 18, wherein the disparity value is calculated by using the decision value stored in the second memory device while the decision value is stored into the first memory device.

21. (Original) The method of claim 19, wherein the disparity value is calculated by using the decision value stored in the first memory device while the decision value is stored into the second memory device.

22. (Original) The method of claim 18, wherein the step of storing comprises the steps of:

initializing a forward processing means according to a base signal;

adding the number of times of an externally inputted clock signal to a number of a processing means used in calculating the decision value; and

calculating a decision value according to the added result.

23. (Original) The method of claim 22, wherein if the added result is an even number, it is determined which signal is active among top and bottom signals, thereby calculating each decision value according to the determination result.

24. (Original) The method of claim 23, wherein if only the top signal is active as a result of the determination, among an up cost, a down cost, and an added cost, the up cost is excluded in comparison objects, then, only the down cost and the added cost are compared to store the minimum cost, and information notifying the minimum cost between the added cost and the down cost is determined as a decision value.

25. (Original) The method of claim 23, wherein if only the bottom signal is active as a result of the determination, among the up cost, the down cost, and the added cost, the down cost is excluded in comparison objects, then, only the up cost and the added cost are compared to store the minimum cost, and information notifying the minimum cost between the added cost and the up cost is determined as a decision value.

26. (Original) The method of claim 23, wherein if neither the top signal nor the bottom signal is active as a result of the determination, the minimum cost is stored among the up cost, the down cost, and the added cost, and information notifying the minimum cost between the up cost, the added cost, and the down cost is determined as a decision value.

27. (Original) The method of claim 22, wherein if the added result is an odd number, `0` is determined as a decision value, and an absolute value of a difference between inputted a pair of image pixel values is added to a stored cost.

28. (Original) The method of claim 18, wherein the step of calculating comprises the steps of:

initializing a backward processing means by a base signal; and

receiving a decision value of an activated processing means, adding the inputted decision value to a previously calculated disparity value, and outputting the added value as a disparity value.